

PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) SiliconStor-03US									
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on _____ Signature _____ Typed or printed name _____	Application Number 10/775,523	Filed 2/9/2004									
	First Named Inventor Sam NEMAZIE et al.										
	Art Unit 2181	Examiner Chun Kuan LEE									
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p> <p>I am the</p> <table style="width: 100%; border: none;"><tr><td style="width: 50%; vertical-align: top; padding: 5px;"><input type="checkbox"/> applicant/inventor.</td><td style="width: 50%; vertical-align: top; padding: 5px; text-align: right;">_____ /Maryam Imam/ Signature</td></tr><tr><td style="vertical-align: top; padding: 5px;"><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</td><td style="vertical-align: top; padding: 5px; text-align: right;">_____ Maryam Imam Typed or printed name</td></tr><tr><td style="vertical-align: top; padding: 5px;"><input checked="" type="checkbox"/> attorney or agent of record. Registration number 38,190</td><td style="vertical-align: top; padding: 5px; text-align: right;">_____ 408-271-8752 Telephone number</td></tr><tr><td style="vertical-align: top; padding: 5px;"><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____</td><td style="vertical-align: top; padding: 5px; text-align: right;">_____ 11/13/2007 Date</td></tr></table> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.</p>				<input type="checkbox"/> applicant/inventor.	_____ /Maryam Imam/ Signature	<input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)	_____ Maryam Imam Typed or printed name	<input checked="" type="checkbox"/> attorney or agent of record. Registration number 38,190	_____ 408-271-8752 Telephone number	<input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____	_____ 11/13/2007 Date
<input type="checkbox"/> applicant/inventor.	_____ /Maryam Imam/ Signature										
<input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)	_____ Maryam Imam Typed or printed name										
<input checked="" type="checkbox"/> attorney or agent of record. Registration number 38,190	_____ 408-271-8752 Telephone number										
<input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____	_____ 11/13/2007 Date										
<input checked="" type="checkbox"/> *Total of 4 forms are submitted.											

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant: Sam Nemazie et al. Docket No: Siliconstor-0003US

Serial No: 10/775,523 Group Art Unit: 2181

5 Filing Date: 02/09/2004 Examiner: Lee, Chun Kuan

Confirmation No.: 1041 Customer No.: 27728

For: "Route Aware Serial Advanced Technology Attachment (SATA) Switch"

Mail Stop AF

Commissioner for Patents

10 P.O. Box 1450

Alexandria VA 22313-1450

STATEMENT IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

15 A Pre-Appeal Brief Request For Review, with appropriate fees, is being submitted herewith because on 10/15/2007, independent claims 1, 9, 14, and 19 and all claims depending therefrom, were rejected under 35 U.S.C. 103(a), on the grounds that the claimed invention is allegedly obvious over US Patent 6,961,813 (hereinafter "Grieff") in light of U.S. Publication No. 2003/0131166 A1 (hereinafter "Utsunomiya").

20 Applicants maintain that the claimed invention is patentable over Grieff in light of Utsunomiya. The test for obviousness has not been properly applied because: the proposed combination of references simply will not work; the references do not teach, suggest or hint at the invention, as claimed; a *prima facie* showing of obviousness has not been made; hindsight has been used to reconstruct the claimed invention, and the references are non-analogous art.

25 *A. The proposed combination of references simply does not work.*

30 The Office Action of August 10, 2007 states that "it would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Utsunomiya's task file queue into Grieff's ATA ports for the benefit decreasing the work load of the host unit for issuing commands." Office Action of August 10, 2007, page 9. It is not clear whether a single task file queue (TFQ) 16 of Utsunomiya is being split into the host ports 130, 132 of Grieff or whether the TFQ 16 is replicated with each TFQ being placed into one host port 130, 132.

Assuming the former, the TFQ 16 of Utsunomiya is split into two separate TFQs each with half the capacity of the whole TFQ, reducing queuing functionality. Assuming the latter, the combination (hereinafter "speculated combination") does not work.

The speculated combination will not work because, in Grieff, the host ports 130 and 132 are Link Layer (layer 2) state machines for relaying primitives with no mention of storage capability.

Grieff: Col. 5, lines 50-56. It is noted that SATA uses a multi-layer communication protocol with four layers, each with different functionality. SATA Specification ver. 2.6 (February 15, 2007) 42-43. To properly interact, components must operate on the same layer: a component operating on the Link Layer (layer 2) cannot operate on the Command Layer (layer 4). SATA Specification ver. 2.6 (February 15, 2007) 42-43.

Thus, the host ports 130, 132 of Grieff cannot interface with the TFQs from Utsunomiya which function at the Parallel ATA (PATA) Application Layer. Furthermore, the arbiter module 112 of Grieff, processes at the Link Layer (layer 2) rather than the Command Layer (layer 4). [See: Grieff, Col. 5, Lns. 50-56]. Even assuming *arguendo* that the arbiter module of Grieff can be redesigned to work in layer 4, redesigning the arbiter module 112 would in turn require re-engineering each subsequent component to interact with Command Layer (layer 4) at the host ports 130, 132. It is not clear whether any of the above reengineering will even work. Accordingly, the speculated combination cannot “concurrently access the device by accepting commands, from either ... host unit, at any given time, including when the device is not in an idle state,” as recited in claims 1, 9, and 14. [See also Amendment filed on October 5, 2007, pg. 9].

Specifically, in the claimed invention, the first and second task files are each separately responsive to commands from the first and second host units, respectively. Thus, they concurrently accept commands, even when the device is non-idle. In the claimed invention, arbitration is not performed until after commands have been stored in the task files. As claimed,

“a first serial (SATA) port including a first host task file responsive to a non-data (FIS) from a first host unit; a second SATA port including a second host task file, responsive to a non-data FIS from a second host unit; a third SATA port, responsive to a non-data FIS from a device; and an arbitration and control circuit for selecting one of the...host units to concurrently access the device, through the switch, by accepting non-data FIS, from either...host unit, at any given time, including when the device is not in an idle state.” [Claims 1, 9, and 14]

The foregoing is in sharp contrast with the speculated combination wherein the arbiter module 112, processing on the Link Layer (layer 2) cannot distinguish between command and data FIS. Grieff: Col. 5, Lns. 50-53. The command in the speculated combination is only decoded when it reaches the FIS decoder 120 in Grieff. The arbiter module 112 in Grieff appears to identify a host for exclusive access to the device. When one host has won arbitration, it has exclusive access to send a command to the dual port adaptor. The other host

must wait until the command is completed and the device is idle to send a command. [See Grieff: Col. 5, Lns. 56-62 and Col. 7, Lns. 2-6. See also Amendment filed on October 5, 2007, at page 8].

Thus, the speculated combination does not work, nor allows for concurrent access by the two host units. Furthermore, neither Grieff nor Utsunomiya suggests, hints at or teaches the speculated combinations.

The standard for obviousness analysis is set forth in *KSR International Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (2007). In *KSR*, the Court held that "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art...Inventions in most, if not all, instances rely upon building blocks long since uncovered and claimed discoveries almost of necessity will be combinations of what . . . is already known." *Id.* at 1741. Obviousness may be found where "a patent for a combination . . . only unites old elements with no change in their respective functions." *Id.* at 1739. The Court held that an invention is obvious where "a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." (emphasis added) *Id.* at 1742.

Under *KSR*, the mere fact that the claimed invention contains parts that existed in the prior art does not automatically render it obvious. Accordingly, the combination of elements from Grieff and Utsunomiya cannot simply be put together like a puzzle to yield the claimed invention. That is, the TFQs of Utsunomiya cannot just be located within the structure of Grieff.

B. The references do not set forth an apparatus/method for making the routing of non-data FIS transparent to the switch.

The claimed invention recites that "the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch." Claims 1, 9, 14, and 19.

The Office Action dated August 10, 2007 erroneously states that "Grieff further teaches said switch comprising wherein a bit is used to indicate which host is the origin or destination of the non data FIS (Grieff, Col. 4, ll. 47-57 and col. 10, l. 27 to col. 12, l. 29) as each non-data FIS comprise an associated 5-bit tag utilized for identifying which host is the origin or destination of the FIS." Office Action dated August 10, 2007, page 10, paragraph 15. The rejection points to two different portions of Grieff. Each is discussed separately hereinbelow.

1- Grieff, Col. 4 ll 47-57: It is Applicants' understanding that this citation misconstrues Grieff. These cited discussions relate to "an ATA device that supports command queuing (of)

PACKET, READ DMA QUEUED, and WRITE DMA QUEUED commands.” (Grieff, ll.47-48). Command queuing is an optional functionality provided for in SATA., as discussed in SATA Rev 2.6 specs, “13.5 Native Command Queuing (Optional).” SATA devices offering this optional SATA feature can queue up to 32 commands internally. [*Id.*]

5 Grieff states that it supports the SATA Queued Command feature. Grieff Col. 4, ll. 38-40. In Grieff, a host “issuing a queued command...places a unique Tag in bits 7-3 of the ATA Sector Count register.” Grieff, Col. 4, ll. 53-55. This “5-bit tag assigned from the host (serves) to uniquely identify a specific command completion when the device completes queued commands out of order.” Grieff Col. 4, ll 51-53. But the Final Office Action of August 10, 2007, erroneously
10 states that the “associated 5-bit tag (is) utilized for identifying which host is the origin or destination of the FIS.” Final Office Action of August 10, 2007, page 10, paragraph 15.

 Therefore, although this 5-bit tag is used to identify queued commands, the Final Office Action erroneously concludes that they are used to identify the host.

2- Grieff, Col. 10, l. 27 to col. 12, l. 29: These discussions actually show the claimed
15 invention is absent in Grieff. The claimed invention uses “non-data FIS...(to) identify which...host unit is an origin and/or destination host so that routing of non-data FIS is transparent to the switch.” (claims 1, 9, 14, and 19) In contrast, Grieff uses an Outstanding Request (OR) Table 116, in combination with a Command Tracker State Machine (SM) 114 to route the non-data FIS to the appropriate host.

20 In Grieff, “When the Command Tracker detects an incoming queued command from the host side interface of the dual port adapter, a new Tag is assigned to the command to guarantee uniqueness of Tags between multiple initiator commands.” Grieff, Col. 10, ll 18-31. “The information stored in the OR_Table may include...the host that sent the command.” Grieff, Col. 10 ll. 42-46. The “In an exemplary embodiment, OR_Table 116 includes a data table that stores...the
25 originating source of each outstanding command” Grieff Col. 5 l. 67 to Col.6 l. 4. “The Command Tracker SM takes measure to determine the correct host to reconnect to if the D_Status[SERV] bit is set.” Grieff, Col. 11, ll 54-56.

 In short, whereas the claimed invention uses the non-data FIS itself “so that routing of non-data FIS is transparent to the switch” (claims 1, 9, 14, 19) Grieff assigns a Tag to the commands,
30 which may be stored in an OR_Table, and is kept track of by the Command Tracker SM.

C. A prima facie basis for obviousness rejection has not been made.

In re Kahn, 441 F.3d 977 (Fed. Cir. 2006) sets forth the requirement for a *prima facie* showing of obviousness. Under *Kahn*, a *prima facie* case is made where “both the scope and content of the prior art and [the] level of ordinary skill in the pertinent art” are considered. *Id.* at 986. Because the rejection doesn’t address the “ordinary skill in the pertinent art” standard, the *prima facie* showing of obviousness has not been made.

D. Improper Hindsight was used to Determine that the Claimed Invention was Obvious

The use of hindsight to reject an application as obvious is impermissible. *KSR*, 127 S. Ct. at 1742. Since the office actions, to date, do not address the level of ordinary skill in the art, an inference is created that hindsight was used to find obviousness. *In re: Kahn* at 986.

It is recognized that “any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight, but so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made and does not include knowledge gleaned only from applicant’s disclosure, such reconstruction is proper” *In re McLaughlin*, 443 F.2d 1392, 1394 (CCPA 1971). Here, as noted, the speculated combination simply does not work. Furthermore, the claimed invention is so far beyond the speculated combination so as to exceed the ordinary creativity of one skilled in the art. Therefore, it is clear that the claimed invention was not viewed from the state of the art when it was created, but rather the claimed invention itself is being used to justify a determination of obviousness. This is improper use of hindsight and should be disregarded for purposes of evaluating the claimed invention.

E. Utsunomiya and Grieff are Non-Analogous Art

Grieff and Utsunomiya are non-analogous art because they purportedly comply with SATA and PATA standards, respectively. The former deals with serial data transfer while the latter deals with parallel data transfer. Specifically, SATA operates serially at 1.5Ghz and 3Ghz (generation 1 and 2, respectively), using 8b/10b encoding, in a four-layer architecture. SATA Specification ver 2.6 (February 15, 2007) 42-43. PATA, however, sends transfer data in parallel, in a one-layer architecture. Reply to Non-Final Office Action 2/21/2007 at pg 14.

In conclusion, the claimed invention is non-obvious because the speculated combination simply will not work; the speculated combination does not teach, suggest or hint at the invention, as claimed; a *prime facie* showing of obviousness has not been made, hindsight has been used to reconstruct the claimed invention, and the references are non-analogous art.